DELAY-MATCHED ASIC CONVERSION OF A PROGRAMMABLE LOGIC DEVICE

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ABSTRACT

An ASIC conversion of a programmable logic device (PLD) is provided. The PLD includes a plurality of logic blocks coupled together by a PLD routing structure. The ASIC includes a plurality of logic blocks corresponding on a one-to-one basis with logic blocks in the PLD and a routing structure corresponding to the programmable routing structure of the PLD. Vias or traces are selectively placed in the ASIC so that logical behavior of its logic blocks matches that implemented in the PLD and the signal propagation delay through the ASIC matches the delay through the PLD.